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(71) Applicant: SHARP KABUSHIKI KAISHA
Osaka 545 (JP)

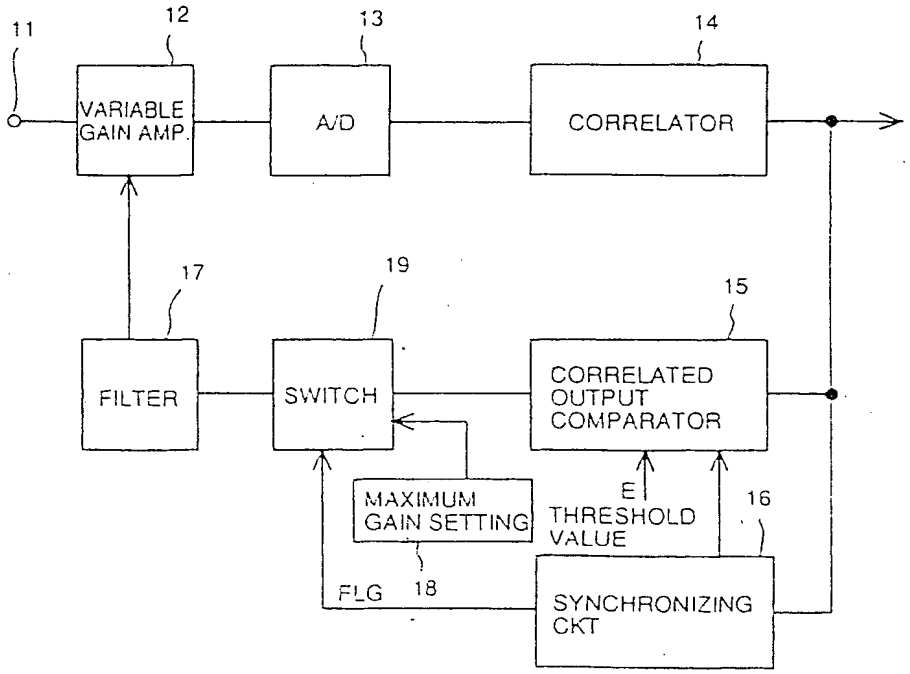
(72) Inventor: Okamoto, Naoki
Chiba-shi, Chiba (JP)

(74) Representative: Brown, Kenneth Richard et al
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

## (54) Spread spectrum signal receiver

(57) Amplitude level of a received signal is controlled by a variable gain amplifier (12), the received signal with the amplitude level controlled is converted to a digital signal by an A/D converter (13), and correlation or demodulation is established by a correlator (14) on the digital value. A correlated output comparator (15) compares an output signal from the correlator with a prescribed threshold value to establish correlated synchronization using the output signal from the correlator, performs initial synchronization using the comparison output, the output amplitude level of the variable gain amplifier (12) is controlled in accordance with an output amplitude from the correlator (14), and gain of the variable gain amplifier (12) is switched to the maximum value by a switch (19) dependent on presence/absence of a synchronization establishment signal from the correlation synchronizing circuit (16).

FIG. 4

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## Description

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The present invention relates to a spread spectrum signal receiver. More specifically, the present invention relates to a spread spectrum signal receiver in which data spectrum is spread by a spread code and transmitted in broad band.

#### Description of the Background Art

Communication using narrow band modulation system has been conventionally used in the field of data communication. Such a system is advantageous in that demodulation at the receiver can be carried out by a relatively small circuitry. However, it has a disadvantage that performance degrades because of multipath fading in an environment having multiple paths such as in a room (office, factory or the like).

By contrast, in spread spectrum communication system, spectrum of data is spread by a spread code and the data is transmitted in a broad band. Therefore, it is resistant against such frequency selective fading, and therefore the aforementioned disadvantage of narrow band communication can be eliminated. In order to implement digital processing in such a system, an A/D converter is used so that the data is converted and processed in the form of digital signals.

A conventional example of the receiver will be described with reference to the block diagram of Fig. 1. A signal from an input terminal 1 is amplified by a variable gain amplifier 2, passed through an A/D converter 3 and input to a correlator 4. An output from correlator 4 is input to a synchronizing circuit, and correlation synchronization is established at the correlated timing. By using a correlation synchronization pulse indicating the correlated and synchronized timing, the correlated output at that time is compared with an optimally set threshold value by a correlated output comparator 5, the output from comparison is smoothed by a filter 7, and thereafter it is applied to variable gain amplifier 2 so that the gain is controlled. In this manner, the maximum point where correlated output matches (hereinafter referred to as correlation spike) is always kept constant.

In order to fully make use of the performance of the receiver, the desired signal level to be input to A/D converter 3 has an optimal value, and it is not the case that any signal level may be input. The optimal value is known as the optimal quantization interval and in accordance with this interval, the signal amplitude of the input to A/D converter 3 must be optimized by means of variable gain amplifier 2. However, it is difficult to control the amplitude of the signal input to A/D converter 3 to be optimal by variable gain amplifier 2. Therefore, instead, correlation spike is controlled such that it is kept constant.

If optimal signal amplitude is established, the amplitude of the correlation spike is constant. In other words, by controlling the gain of the variable gain amplifier 2 such that the amplitude of correlation spike is kept constant, the input signal comes to have an optimal amplitude, that is, optimal quantization interval is obtained, and hence the receiver comes to have best performance.

The operation in a steady state period will be described with reference to Figs. 2A to 2C. In correlated output comparator 5, correlation spike P shown in Fig. 2A is compared with a threshold value E which is set in advance. Amplitude of correlation spike P varies from time to time. Meanwhile, the threshold value E is the optimal amplitude of the correlation spike. By comparing these two, a difference signal is output. The difference signal is as shown in Fig. 2B. By filtering the difference signal by a filter 7, a waveform shown in Fig. 2C is obtained. The waveform is determined by a constant of filter 7.

The filter 7 is to average variation caused by noise. By controlling variable gain amplifier 2 using thus obtained output, the gain of amplifier 2 is lowered when correlated spike P is larger than the threshold value E, and the gain of amplifier 2 is increased when correlation spike P is smaller than the threshold value E. Feedback control is thus realized, whereby the peak of the correlation spike P is kept always matching the set threshold value E.

However, at the start of communication, correlation is not established. Therefore, the correlation synchronization pulse from synchronizing circuit 6 is generated not at the correct position of the correlation spike P. Therefore, in that case, correlated output compactor 5 compares the output with the threshold value E regardless of whether it is a correlation spike or not, and using the resulting difference signal, the variable gain amplifier 2 is controlled.

Now, let us consider the operation of the synchronizing circuit 6. In synchronizing circuit 6, of an initial synchronizing circuit and a synchronization protecting circuit constituting the synchronizing circuit 6, first, the initial synchronizing circuit operates to establish synchronization. Thereafter, synchronization is maintained by the synchronization protecting circuit. In this manner, correlation synchronization pulse point is controlled such that it always appears at the correlation spike P. The initial synchronizing circuit compares an input signal with a set threshold value (the threshold provided for the synchronizing circuit 6 and not shown in Fig. 1), and if the input signal is higher, it assumes that the input signal is the correlation spike P. By repeating this operation several times at the same timing, synchronization is established.

However, in the conventional example, before initial synchronization is established, amplification rate of the variable gain amplifier 2 is unknown, and hence the sig-

nal amplitude entering A/D converter 3 is also unknown. This means that the amplitude of correlation spike P is also unknown. This makes it difficult to set the threshold value of the initial synchronizing circuit. Accordingly, there is a method for initial synchronization in which variable gain amplifier 2 is subjected to automatic gain control (AGC) so that the output signal from variable gain amplifier 2 is kept constant.

Fig. 3 shows this structure. Basically, this structure is the same as Fig. 1, except that an AGC circuit 8 is provided at the output of variable gain amplifier 2 for detecting power from the output and for keeping constant the amplitude. AGC circuit 8 is equivalent to any AGC circuit used in general communication equipment. In the structure shown in Fig. 3, at the time of initial synchronization, a switch 9 is switched so that the amplitude of the output from variable gain amplifier 2 is kept constant by the output from AGC circuit 8, and after initial synchronization is established, the variable gain amplifier 2 is controlled referring to the correlated output as shown in Fig. 1. This switching is performed using a synchronization flag FLG output from synchronizing circuit 6, indicating whether or not initial synchronization is established.

However, the conventional circuit is disadvantageous in that it requires additional AGC circuit 8. Though AGC circuit 8 can be implemented by a capacitor or a diode for detection, an analog filter or the like, these elements are all analog devices having large circuit scale and not suitable for integration.

## SUMMARY OF THE INVENTION

An object of the present invention is to provide a spread spectrum signal receiver having a simple structure and capable of stably performing initial synchronization.

Briefly stated, in the present invention, the received signal is amplified by a variable gain amplifier, an output signal from the amplifier is converted to a digital signal by a converting circuit, correlation between the value which has been converted to the digital signal and a spread code is found by a correlator, in order to establish correlated synchronization by using correlated output, a predetermined threshold value and a correlated output are compared by a correlation synchronization circuit so that initial synchronization is established and thereafter synchronization is maintained, level of an output amplitude of the variable gain amplifier is controlled based on the amplitude of the correlator in response to the establishment of synchronization, and gain of the variable gain amplifier is switched to the maximum gain dependent on presence/absence of a synchronization establishment signal.

Therefore, in the present invention, the variable gain amplifier is switched to the maximum gain dependent on presence/absence of the synchronization establishment signal, so that the signal amplitude at the time of initial synchronization can be kept at the maximum value.

In a preferred embodiment, a holding circuit is provided for holding the output amplitude value output from the gain control circuit while the synchronization is maintained as a gain control value, and the gain of the variable gain amplifier is controlled by the held gain control value. Therefore, in this embodiment, when the synchronization establishment signal is generated from correlation synchronizing circuit, the control value held from the maximum gain can be set again, and therefore at the time of air link disconnection, a value before disconnection can be readily recovered.

In a more preferred embodiment of the present invention, the gain control value held by the holding circuit is resettable. Therefore, in the preferred embodiment, the value is not always returned to the state before disconnection but it can be changed in accordance with an instruction from an upper layer, such as a protocol.

More preferably, a filter for smoothing the output from the gain control circuit is provided, and the time constant of the filter is made variable. Therefore, in the more preferred embodiment, time for convergence to the transitional state period can be made shorter by varying the time constant.

Further, in a more preferred embodiment, by changing the threshold value in a transitional state in the correlation synchronizing circuit, the performance of the synchronization protecting circuit in the transitional state can be improved.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit block diagram showing a conventional example.

Figs. 2A to 2C show operation of the conventional example, showing a correlated output, a comparison output and a filter output.

Fig. 3 is a circuit block diagram showing a conventional example.

Fig. 4 is a circuit block diagram showing an embodiment of the present invention.

Figs. 5A and 5B show quantization of A/D converter in accordance with an embodiment of the present invention.

Fig. 6 is a circuit block diagram showing an embodiment of the present invention.

Figs. 7A and 7B show control voltage of the variable gain amplifier in accordance with the embodiment of the present invention.

Fig. 8 is a block diagram showing an embodiment of the present invention.

Figs. 9A and 9B show control voltage of the variable

gain amplifier in accordance with the embodiment of the present invention.

Fig. 10 is a circuit block diagram showing an embodiment of the present invention.

Fig. 11 is a circuit block diagram showing an embodiment of the present invention.

Fig. 12 shows control voltage of the variable gain amplifier in accordance with the embodiment of the present invention.

Fig. 13 is a circuit block diagram showing an embodiment of the present invention.

Fig. 14 is a circuit block diagram showing an embodiment of the present invention.

Fig. 15 shows amplitude of the correlated output.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the present invention will be described with reference to Fig. 4. This is a circuit block diagram showing the structure of the receiver. A signal from input terminal 11 is amplified by variable gain amplifier 12, converted to a digital signal by A/D converter 13 and input to correlator 14. An output signal from correlator 14 is input to correlated output comparator 15 as well as to synchronizing circuit 16.

In synchronizing circuit 16, correlated synchronization is established at the correlated timing. By using the correlated synchronized pulse indicating the correlated and synchronized timing, the correlated output at that time and an optimally set threshold value E are compared by correlated output comparator 15 (compared and a difference signal therebetween is output). At this time, synchronization flag FLG output separately from synchronizing circuit 16 indicates synchronization. Therefore, switch 19 is switched such that the signal from correlated output comparator 15 is selected, in accordance with the flag FLG.

Accordingly, the comparison output from the correlated output comparator 15 controls, through switch 19 and filter 17, the gain of variable gain amplifier 12. In this manner, when synchronization is established, switch 19 passes the output value obtained by comparison to filter 17, so that the maximum point where correlated output matches (hereinafter referred to as the correlation spike) is always kept constant.

Meanwhile, if initial synchronization is not established, that is, when the timing of the correlation spike is not determined and synchronization flag FLG does not indicate synchronization, switch 19 selects and outputs the value of maximum gain setting circuit 18 and passes it to filter 17. In the first embodiment, as compared with the conventional example shown in Fig. 1, switch 19 and maximum gain setting circuit 18 are necessary. However, these can be implemented in far simpler structure than AGC circuit 3 of Fig. 3.

The reason why initial synchronization can be established by setting the maximum gain will be described. In the present circuit structure, A/D converter 13 is used, which may generally have a resolution of 3 or 4 bits. It may have an analog input range of about 1 to about 2V, which voltage range is divided into 8 or 16 levels.

Such operation is shown in Figs. 5A and 5B. Fig. 5A corresponds to the optimal amplitude. Here, an A/D converter of 3 bits is used, and the input range is divided into 8 levels. As for the magnitude of amplitude, the amplitude having such an amplitude corresponding to the eye pattern shown in the figure provides optimal characteristics. Meanwhile, Fig. 5B corresponds to the maximum amplification of variable gain amplifier 12, in which signal amplitude exceeds 8 levels and all quantized to -7 and 7.

In this case, different from the example of Fig. 5A, not the best performance is obtained with respect to error rate or the like. However, the input signal itself can be quantized to two values, that is, -7 and 7. Therefore, when the signal is spread by using 63 chips, for example, the maximum value of the correlated spike itself will be $63 \times 7 = 441$. Therefore, using this value as a reference, initial synchronization can be performed stably.

In this manner, in the present embodiment, until initial synchronization is established, the gain of variable gain amplifier 12 is set to the maximum, whereby initial synchronization can be performed stably with simple structure as compared with the prior art example. What is done by the maximum gain setting circuit 18 is simply to set the control voltage to the maximum value of variable gain amplifier 12, that is, to a fixed value of 5V, for example. Therefore, as compared with the conventional structure of Fig. 3, the circuit structure is quite simple.

A second embodiment of the present invention will be described with reference to Fig. 6. In Fig. 6, portions corresponding to those of Fig. 4 are denoted by the same reference characters and description thereof is not repeated. In the present embodiment, switch 19 for switching to the maximum gain set value is connected in the succeeding stage of filter 17. In this structure, initial synchronization of correlation is, of course, performed at the start of communication. In addition, initial synchronization of correlation may be necessary dependent on the condition of communicating wireless transceivers, when the air link is disconnected, for example.

In such a case, by the structure shown in Fig. 4, rise of the control voltage of variable gain amplifier 12 is delayed because of the influence of filter 17. The operation of the circuit shown in Fig. 4 is as shown in Fig. 7A. First, synchronization is established, and then air link is disconnected so that synchronization is lost, and synchronization flag indicates off-synchronization at time point t1. Therefore, switch 19 switches to the value of maximum gain. However, because of the integrating characteristic of filter 17, the actual control voltage rises slowly, and attains to the maximum gain after the delay of tD. As a result, reestablishment of synchronization (initial synchronization) is delayed.

However, in the present embodiment (Fig. 6), since there is inserted switch 19 in the succeeding stage of filter 17, the rise of the output from filter 17 is as shown by the dotted line in Fig. 7B while the output from switch 19 is as shown by the solid line in Fig. 7B. Therefore, as compared with the first embodiment, reestablishment is possible in shorter time period. As a result, when the air link is disconnected, the air link can be recovered faster.

A third embodiment of the present invention will be described with reference to Fig. 8. In the figure, portions similar to the second embodiment shown in Fig. 6 are denoted by the same reference characters and description thereof is not repeated. In the third embodiment, there is provided a holding circuit 20 in the preceding stage of filter 17. When flag FLG from synchronizing circuit 16 indicates off-synchronization, holding circuit 20 holds the comparison output from correlated output comparator 15 at that time and when said flag FLG indicates synchronization, applies the held value to filter 17, and in the synchronized state thereafter, passes the output from the correlated output comparator 15 directly to filter 17.

When the air link is disconnected as described above, synchronization flag FLG indicates off-synchronization, and the process for initial synchronization starts. When initial synchronization is established thereafter, the output from filter 17 is again supplied as control signal to variable gain amplifier 12. Difference in operation in that case when holding circuit 20 is provided and not provided will be described with reference to Figs. 9A and 9B.

Fig. 9A shows an example where holding circuit 20 is not provided. When synchronization is lost, the operation is similar to that shown in Fig. 7A, and control voltage is set to the maximum gain. However, when synchronization is reestablished, convergence to optimal value takes time, because of the integrating characteristic of filter 17. In this case, there is a delay of TD2 until convergence to maximum value is completed.

Therefore, in the third embodiment, in order to hold the voltage of the optimal value at the moment when synchronization is lost is held in the holding circuit 20. Therefore, simultaneously with the reestablishment of synchronization, a level close to the optimal value can be obtained. This is shown in Fig. 9B. As a result, the delay tD2 can be made zero, and performance can be improved.

A fourth embodiment of the present invention will be described with reference to Fig. 10. Basically, the structure is the same as the third embodiment described above (Fig. 8). However, in the present embodiment, holding circuit 20 is adapted such that an external reset signal RST can be input through terminal 21. As described with reference to Figs. 9A and 9B, when the air link is disconnected and synchronization is reestablished, convergence to the optimal point is possible at high speed thanks to the holding circuit 20. However, if the disconnected state continues long or at the time of initial synchronization, the value held previously will be meaningless. Therefore, a function of resetting using an external signal is provided.

Though it differs system by system, the reset signal RST may be generated using the length of the disconnected time as a reference, or generated using end of communication of one packet as a reference, by determining end of a data packet based on the demodulated data. In any case, the signal is provided from an upper layer (for example, a signal from a protocol).

A fifth embodiment of the present invention will be described with reference to Fig. 11. In the figure, portions corresponding to those of the second embodiment shown in Fig. 6 are denoted by the same reference characters and description thereof is not repeated. In the present embodiment, a time constant variable filter 17a is used as the filter and variable control thereof is performed by a filter controller 22 which outputs a control signal based on the synchronization flag FLG. The time constant of filter 17a is controlled by filter controller 22 in accordance with the time lapse from establishment of synchronization flag.

At the initial synchronization of correlation, the transitional time is determined by the time constant of filter 17a. At the time of disconnection, optimal value can be recovered quickly by using holding circuit 20 as in the third embodiment (Fig. 8). However, at the time of initial synchronization or when disconnection continues long, the transitional time is still determined by the time constant of filter 17a.

This will be described with reference to Fig. 12. In the conventional filter, as shown by the dotted line in Fig. 12, the transitional characteristic is determined by a time constant which is kept constant normally. Therefore, a time tD3 is necessary to attain the steady state. Further, in the present embodiment, the time constant of filter 17a is switched in the time period t3, steady state can be attained in the time period tD4, and hence the speed of operation can be improved.

In this manner, by the present embodiment, in the initial establishment and in the transitional state, the time constant is set shorter to realize high speed synchronization, while in the steady state, the time constant is set longer to enable stable operation.

Though description was made with reference to Fig. 11, the concept of time constant variable filter 17a and filter controller 22 can be applied to any of the first to fourth embodiments to provide similar effects. Further, the time constant of the filter is switched into two steps in time t3 in the above described embodiment. However, it may be switched in several steps or linearly.

A sixth embodiment of the present invention will be described with reference to Fig. 13. In this embodiment, the comparison output from correlated output comparator 15 is applied not only to filter 17 but also to the synchronizing circuit 16.

The structure of synchronizing circuit 16 is shown in Fig. 14. Synchronizing circuit 16 is divided into initial

synchronizing portion 31 and synchronization protecting portion 32 to which an output from correlator 14 is applied respectively through a terminal 30. When initial synchronization is established in initial synchronizing portion 31, synchronization flag FLG is output, and synchronization protecting process starts. A comparator 31a is provided in initial synchronizing portion 31 by which the level of the correlated output and a prescribed threshold value V1 are compared. When the correlated output is larger than the threshold value V1, initial synchronizing operation takes place.

When initial synchronization is established, flag FLG is set to "1" and synchronization protecting portion 32 is informed of the establishment of the initial synchronization. Thus synchronization protecting portion 32 maintains synchronization, comparing the correlated output from terminal 30 with a threshold value V2. When synchronization is lost, synchronization protecting portion 32 resets itself and also resets the initial synchronizing portion 31. Thus the flag FLG is set to "0." Initial synchronizing portion 31 again performs initial synchronization so as to set flag FLG to "1."

In the synchronizing circuit, separate threshold values are set in initial synchronizing portion 31 and synchronization protecting portion 32, and synchronization is confirmed referring to these threshold values, respectively. Especially in the first to fifth embodiments of the present invention, the gain is maximum at the time of initial synchronization. Therefore, the threshold value is as shown by the threshold value A of Fig. 15, while for protecting synchronization, the threshold value B for the steady state is used.

However, when the operation changes from the initial synchronization to synchronization protecting state, there is a transitional state as described in the embodiments above. Though means for improvement have been proposed, there is still the transitional state. In that case, synchronization protecting portion 32 regards this transitional state as steady state and performs comparison with the threshold value. Therefore, in the above described embodiments, the protecting operation in the transition state may possibly cause error.

Therefore, in the present embodiment, a threshold controller 33 is provided which determines the threshold value in the transitional state using the value of a signal from correlated output comparator 15, and the threshold value is used as the threshold value V2 for the synchronization protecting portion 32. As a result, the threshold value can be controlled as represented by the solid line a in Fig. 15, and correct synchronization protection becomes possible even in the transitional state.

The control is performed in the following manner, for example. If the threshold value in the steady state corresponds to 80% of the correlated output, then the threshold value is set by multiplying the output from correlated output comparator 15 plus amplitude in the steady state by 80%. For the initial synchronizing portion 31, fixed threshold V1 is used similar to the above. This embodiment is applicable to any of the first to fifth embodiments.

As described above, according to the embodiments of the present invention, means for switching the variable gain amplifier to the maximum gain is provided, and therefore the gain is switched to the maximum value dependent on presence/absence of a synchronization establishment signal from the correlation synchronizing circuit. Accordingly, the signal amplitude at the time of initial synchronization can be kept at the maximum value. Since the gain of the variable amplifier is maximized until initial synchronization is established, initial synchronization can be performed stably with simple structure as compared with the prior art, and the circuit structure can be made simpler as compared with the structure shown in Fig. 3 of the prior art example.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

## Claims

1. A spread spectrum signal receiver, comprising:

   variable gain amplifying means (12) for amplifying a received signal;
   converting means (13) for converting an output signal from said variable gain amplifying means to a digital signal;
   correlating means (14) for finding correlation between the value converted by said converting means to the digital signal and a spread code;
   correlation synchronizing means (16) for comparing an output signal from said correlating means with a predetermined threshold value to obtain correlation and synchronization by using the output signal from said correlating means, for performing initial synchronization and synchronization protection after synchronization is established;
   gain control means (15) responsive to establishment of synchronization by said correlation synchronizing means for controlling output amplitude level of said variable gain amplifying means based on an amplitude of said correlating means; and
   switching means (19) for switching gain of said variable gain amplifying means to a maximum gain in accordance with presence/absence of a synchronization establishment signal from said correlation synchronizing means.

2. The spread spectrum signal receiver according to

claim 1, further comprising:

holding means (20) for holding an output amplitude output from said gain control means at the time of synchronization protection as a gain control value; wherein
said variable gain amplifying means has its gain controlled by the gain control value held by said holding means.

3. The spread spectrum signal receiver according to claim 2, further comprising
means (21) for resetting the gain control value held by said holding means.

4. The spread spectrum signal receiver according to claim 1, further comprising
filter means (17) for smoothing an output from said switching means and applying it to said variable gain amplifying means.

5. The spread spectrum signal receiver according to claim 1, further comprising
filter means (17) for smoothing an output from said comparing means and for applying it to said switching means.

6. The spread spectrum signal receiver according to claim 5, wherein

said filter has its time constant made variable (17a), said receiver further comprising
filter control means (22) for changing said time constant in accordance with time lapse from a timing of establishment of said initial synchronization.

7. The spread spectrum signal receiver according to claim 1, wherein

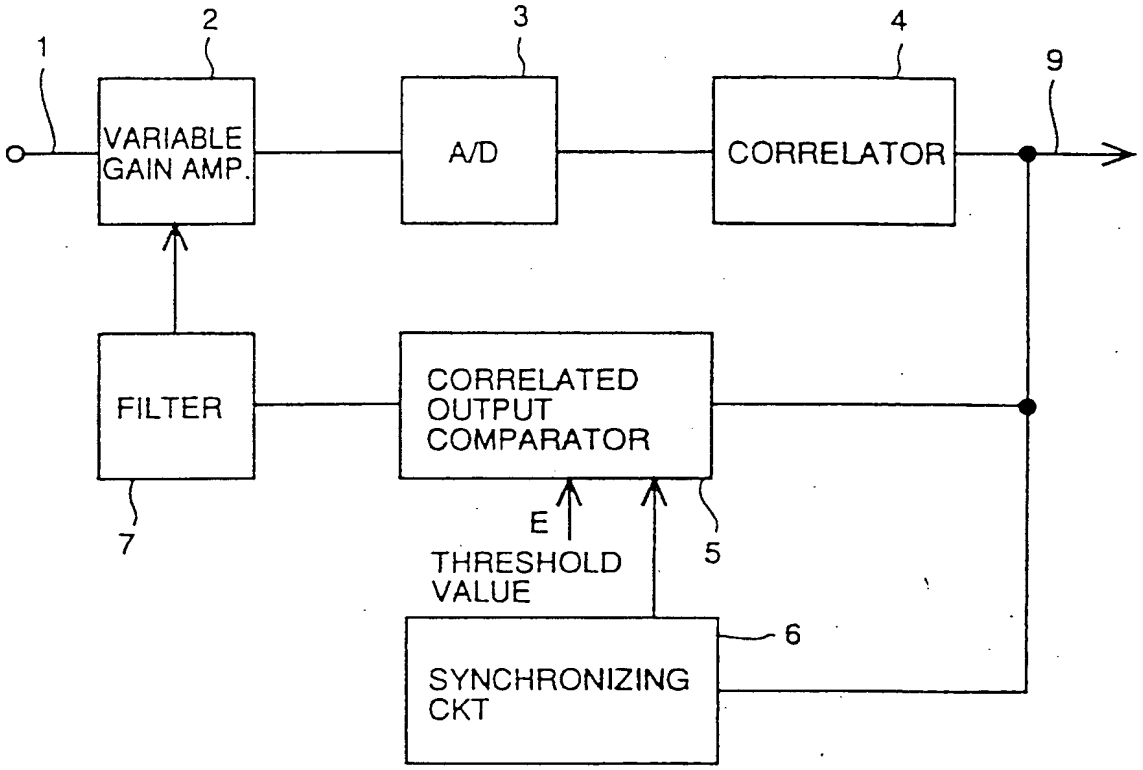
said synchronizing means includes
initial synchronizing means (31) for comparing an output signal from said correlating means and a predetermined first threshold value, for performing initial synchronizing operation when the output signal from the correlating means is larger than said predetermined first threshold value, and
synchronization protecting means (32) responsive to initial operation by said initial synchronizing means for comparing an output signal from said correlating means with a predetermined second threshold value, and for protecting synchronization after synchronization is established when the output signal from said correlating means is larger than said predetermined second threshold value.

8. The spread spectrum signal receiver according to claim 7, further comprising
threshold value control means (33) responsive to an output signal from said gain control means for controlling said predetermined second threshold value of said synchronization protecting means.

9. A spread spectrum receiver comprising

a variable gain amplifier for amplifying a received signal,
a convertor for converting the signal from the amplifier to a digital signal,
means for controlling the gain of the amplifier on the basis of a synchronised, correlated signal obtained from the received signal,
and means for causing the gain of the amplifier to take a fixed, predetermined value when synchronisation is not established.

FIG. 1


1
2
3
4
9
VARIABLE GAIN AMP.
A/D
CORRELATOR
FILTER
CORRELATED OUTPUT COMPARATOR
7
E
THRESHOLD VALUE
5
6
SYNCHRONIZING CKT

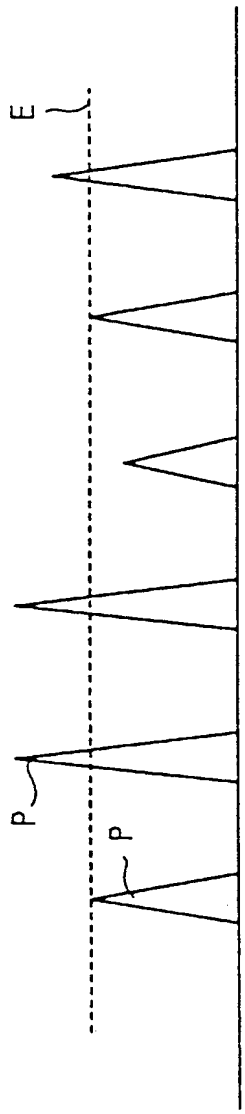



FIG. 2A

CORRELATION SPIKE

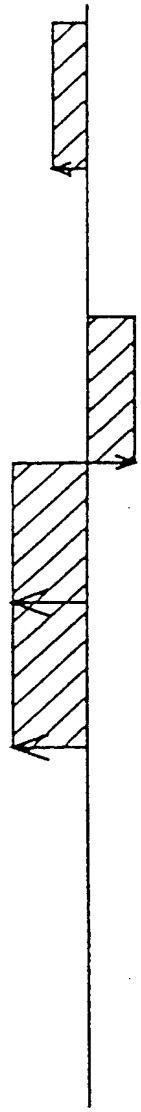


FIG. 2B

OUTPUT FROM CORRELATED OUTPUT COMPARATOR

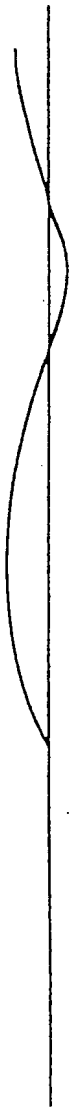


FIG. 2C

FILTER OUTPUT

FIG. 3

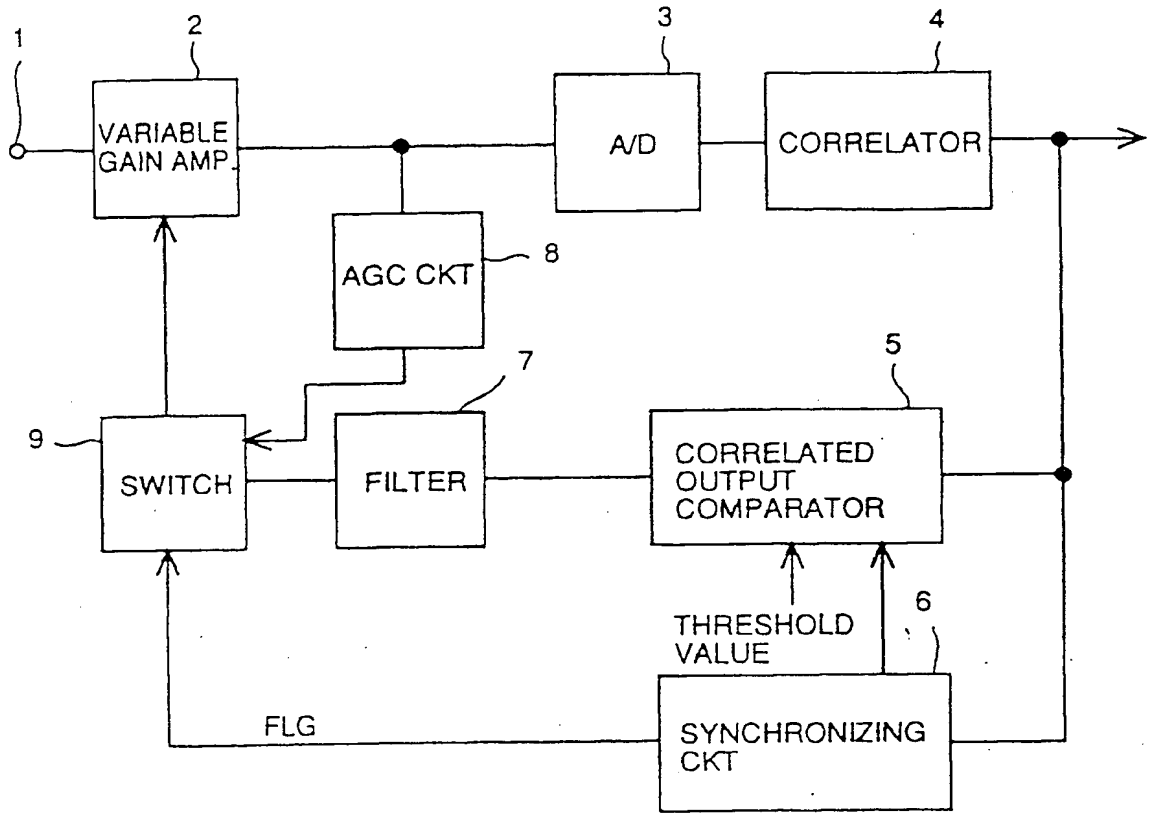


FIG. 4

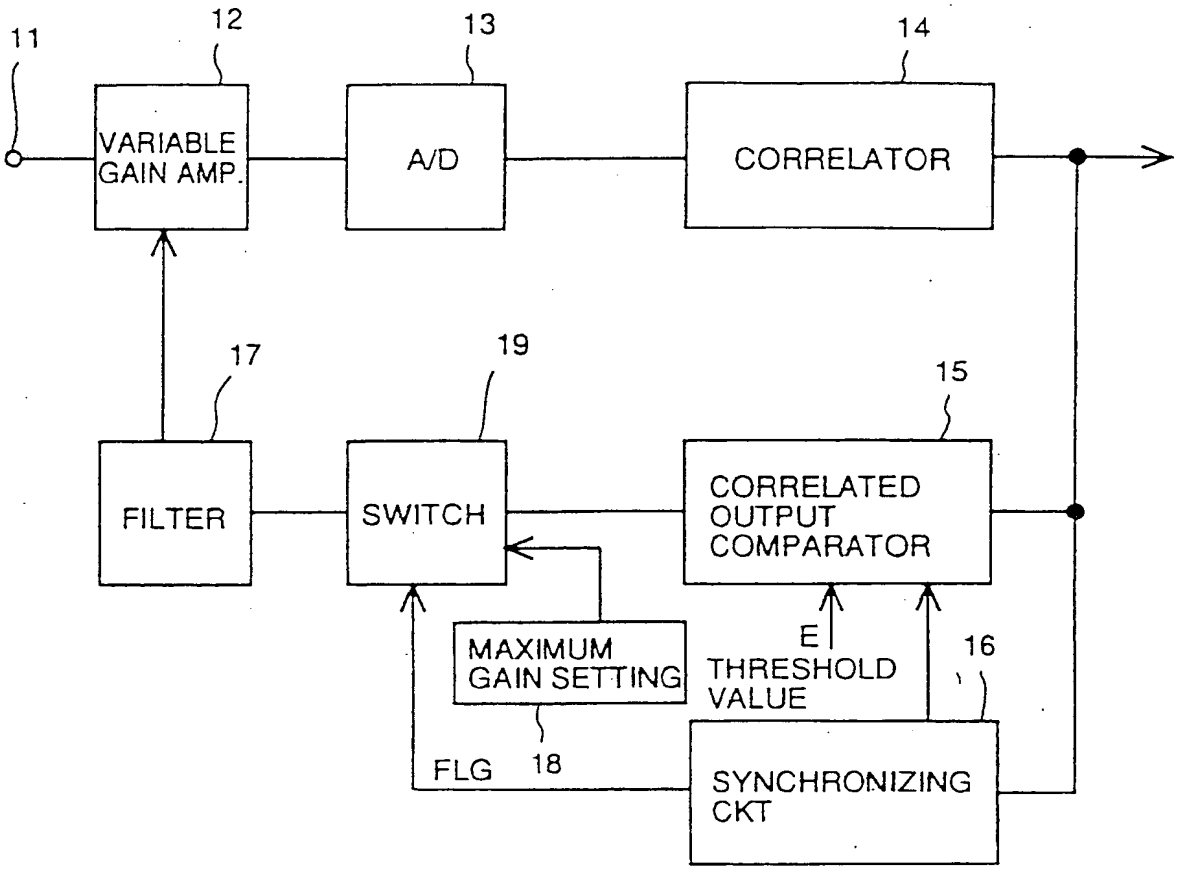


FIG. 5A

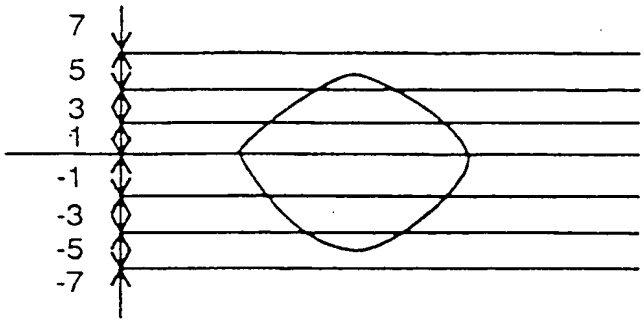



FIG. 5B

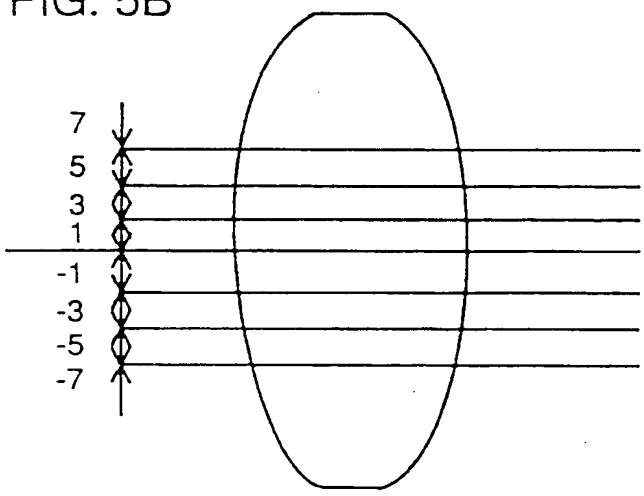


FIG. 6

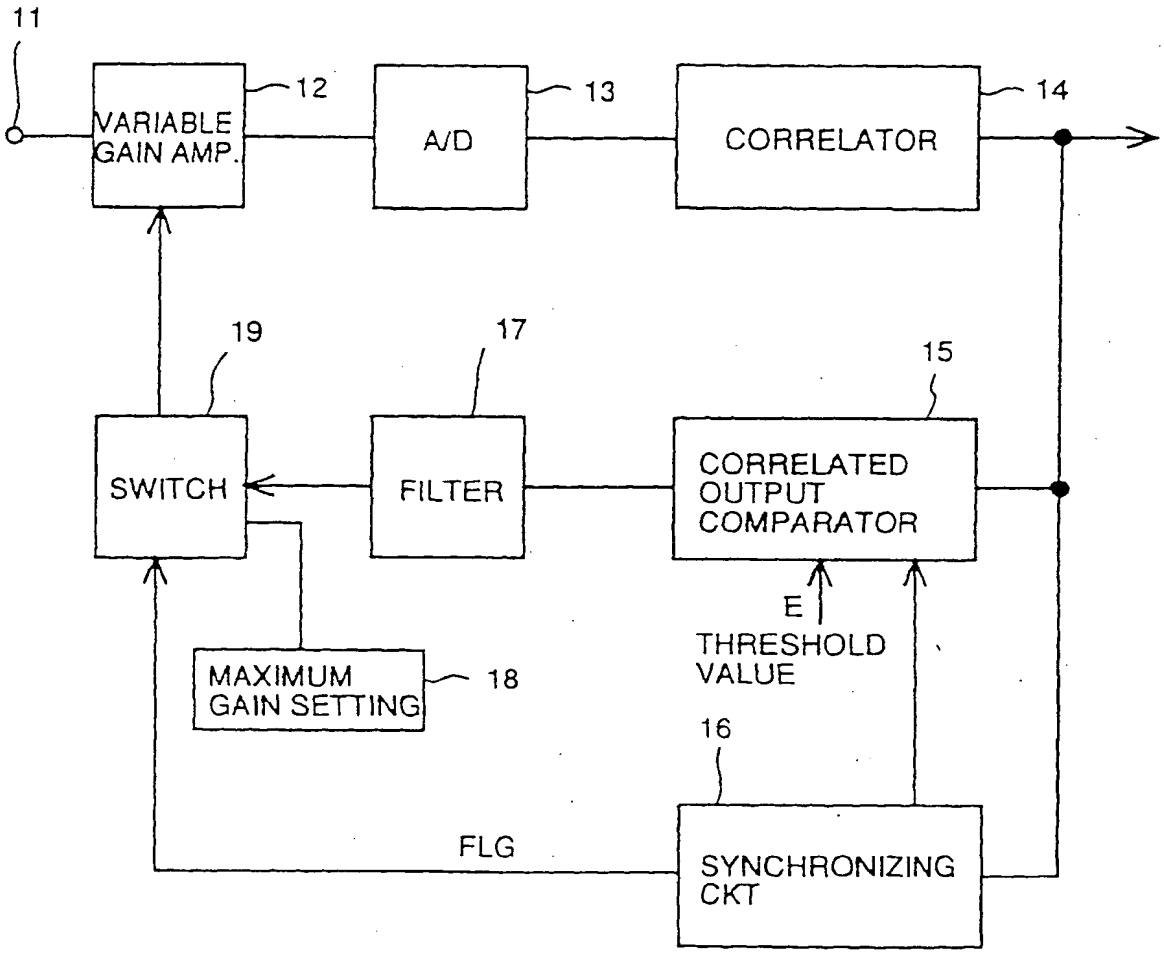


FIG. 7A

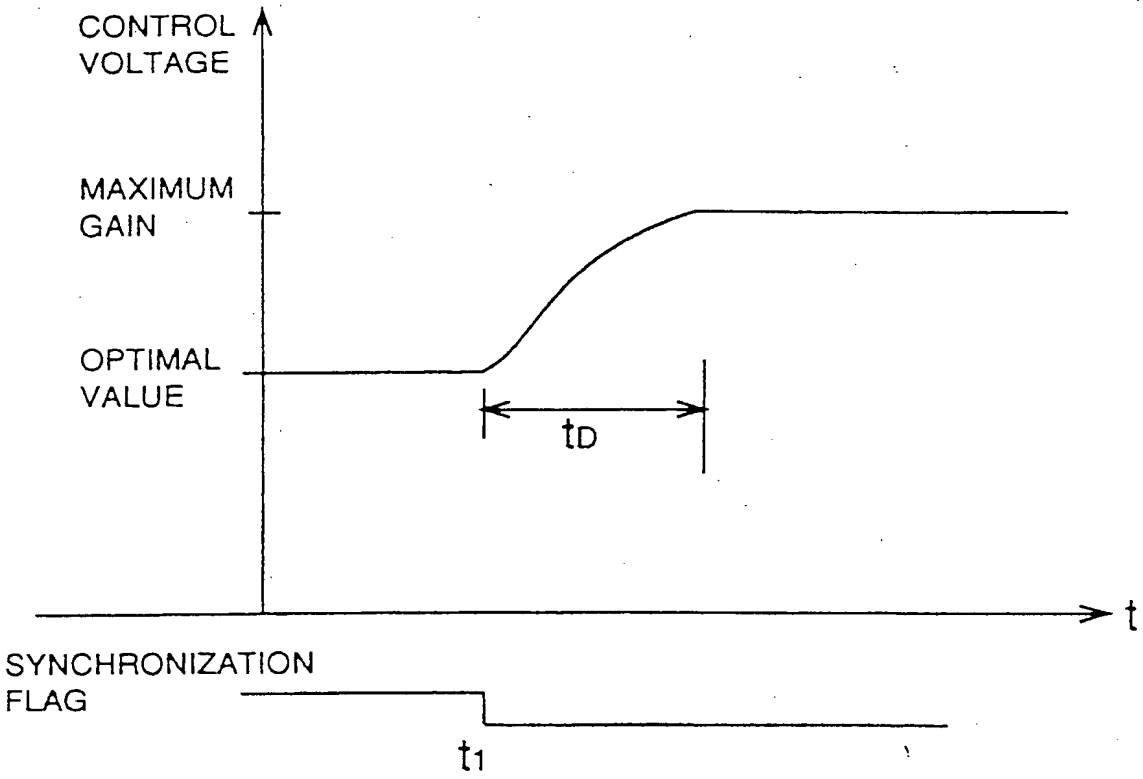



FIG. 7B

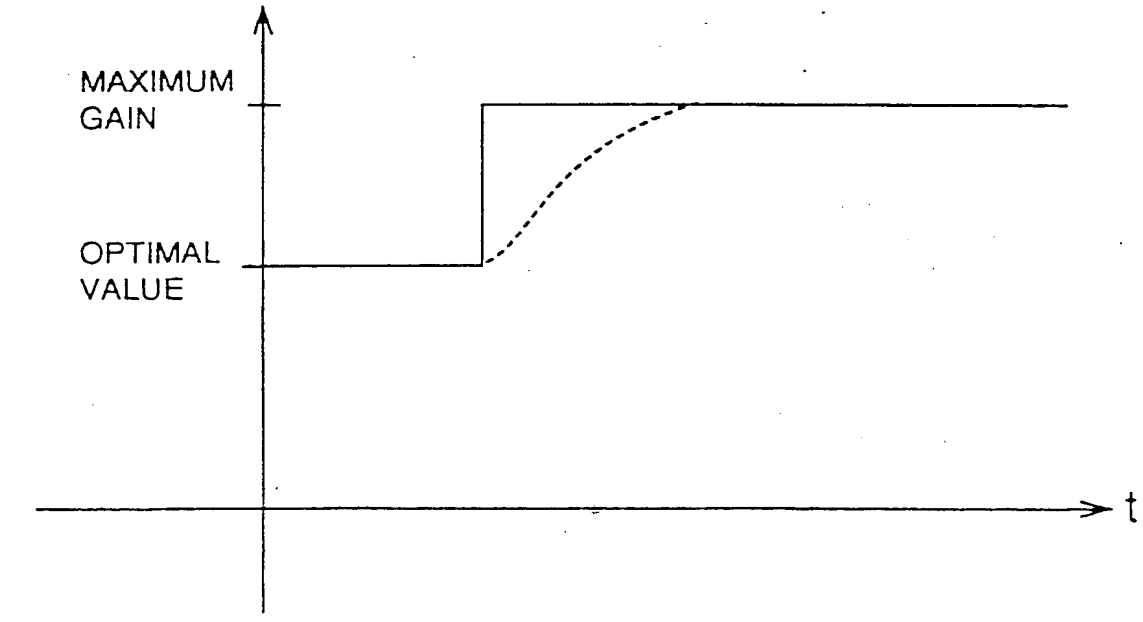


FIG. 8

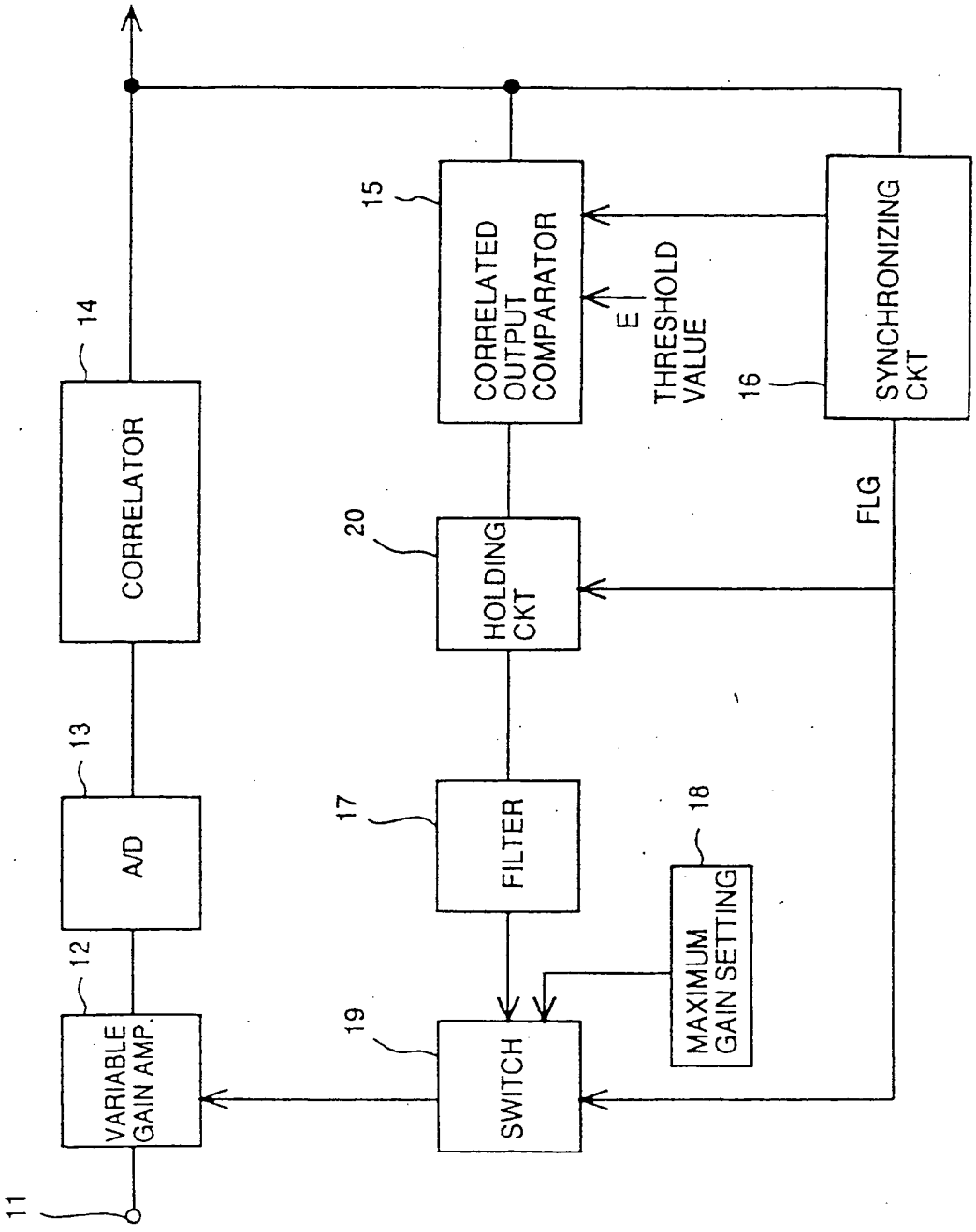


FIG.9A

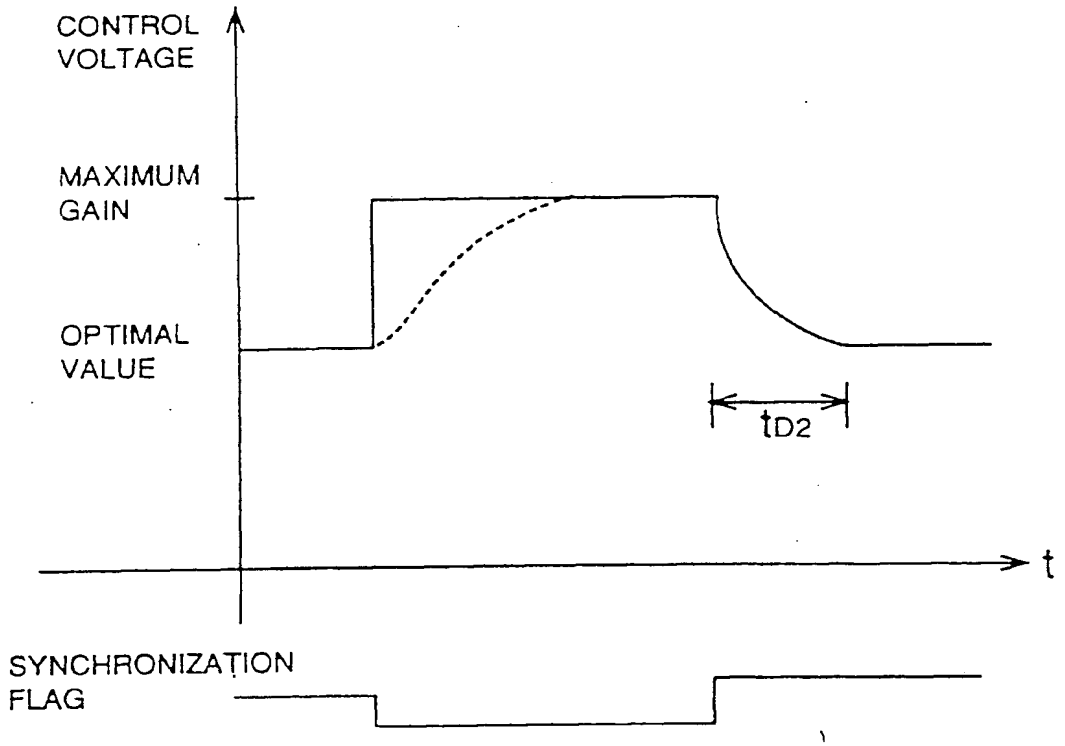



FIG. 9B

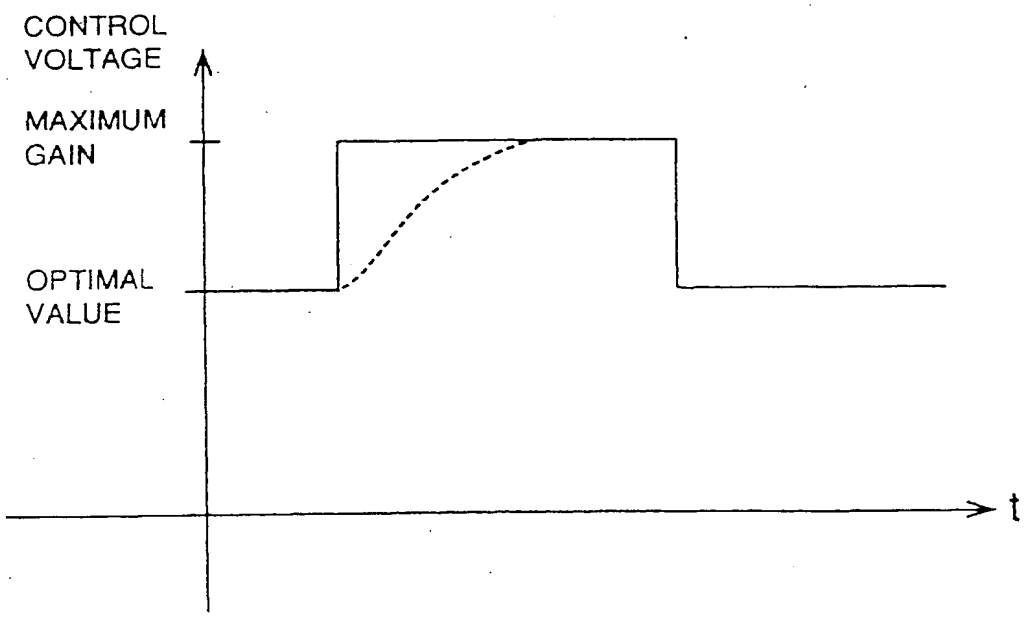


FIG. 10

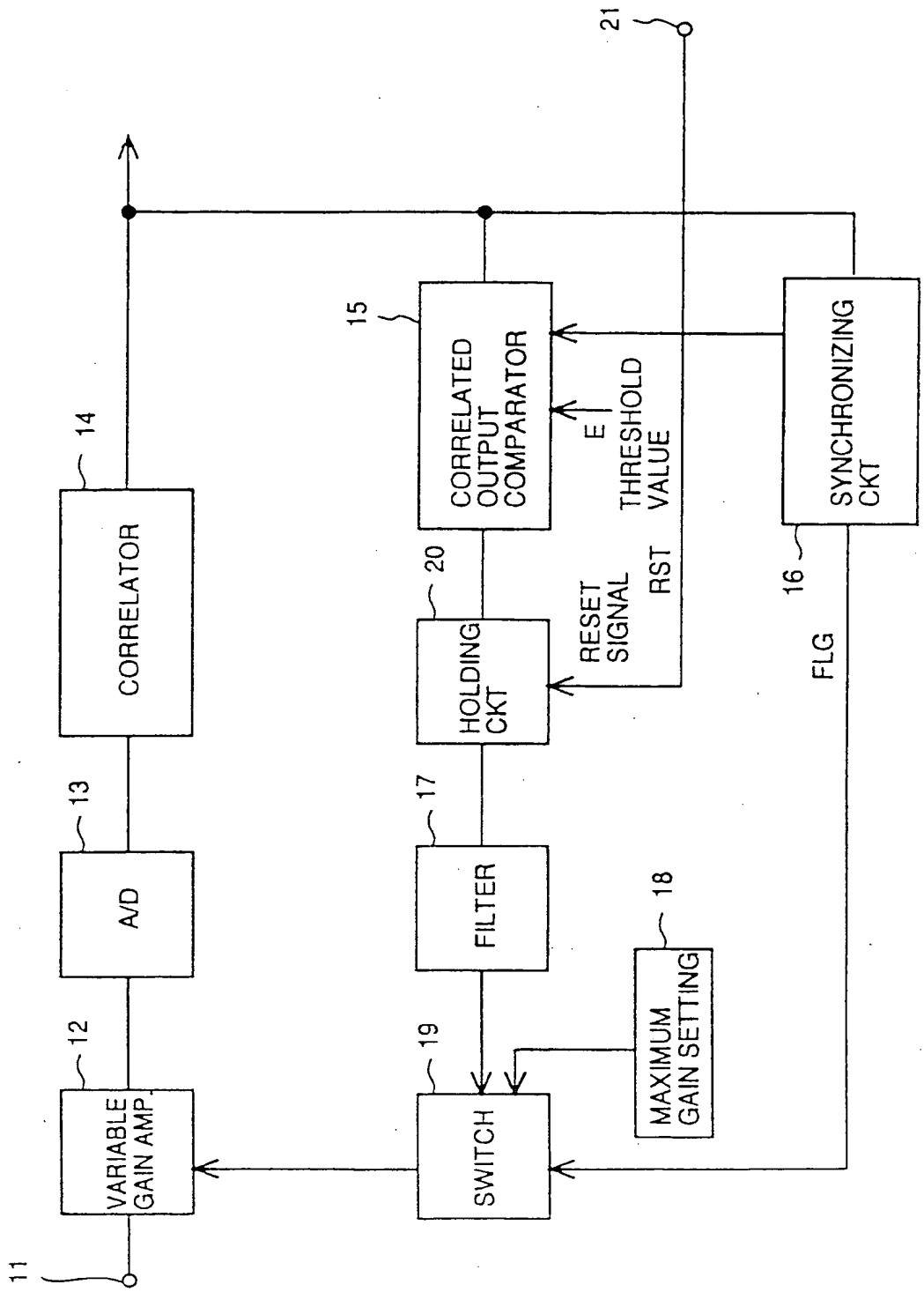


FIG. 11

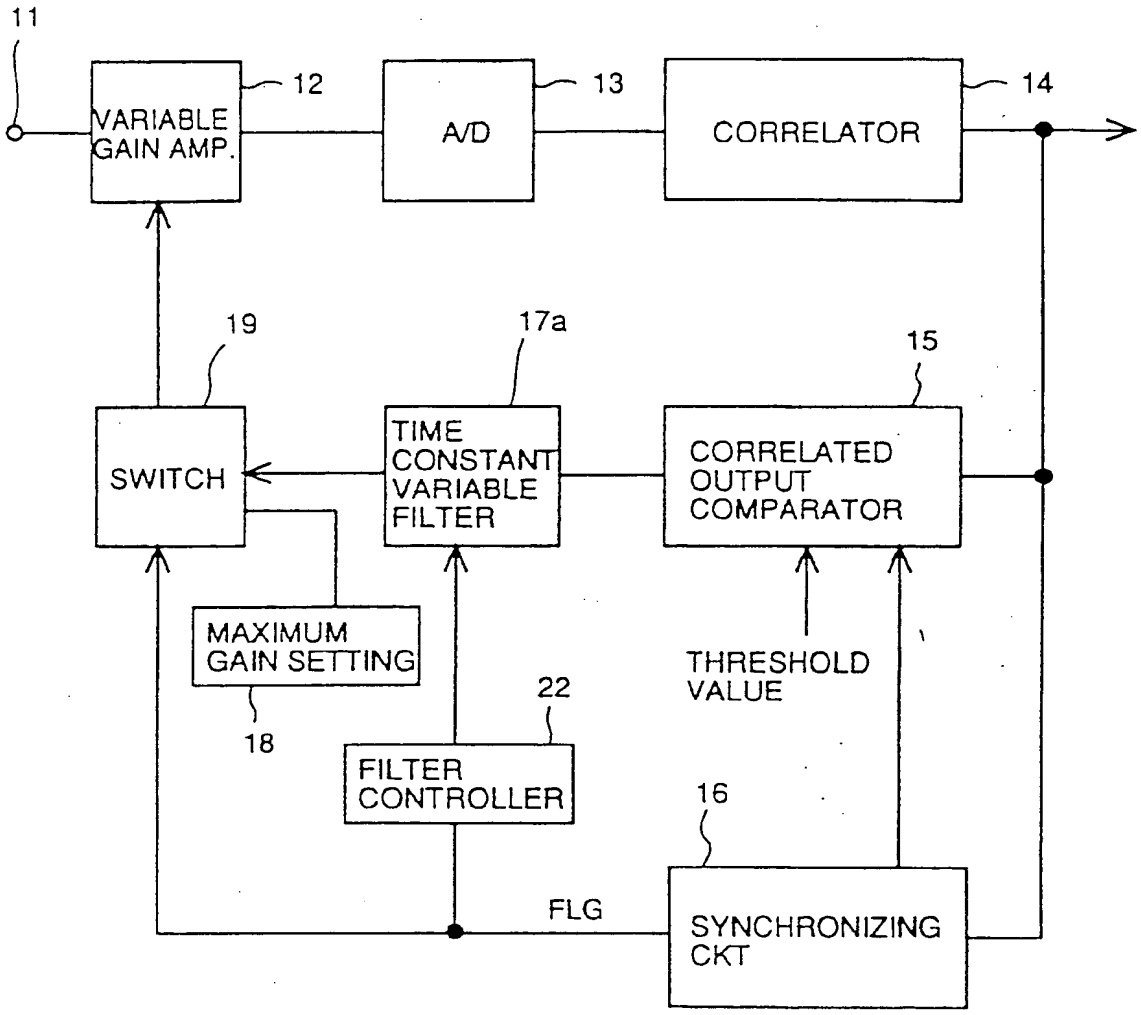

11
VARIABLE GAIN AMP.
12
A/D
13
CORRELATOR
14
19
17a
15
SWITCH
TIME CONSTANT VARIABLE FILTER
CORRELATED OUTPUT COMPARATOR
MAXIMUM GAIN SETTING
18
22
FILTER CONTROLLER
THRESHOLD VALUE
16
FLG
SYNCHRONIZING CKT

FIG. 12

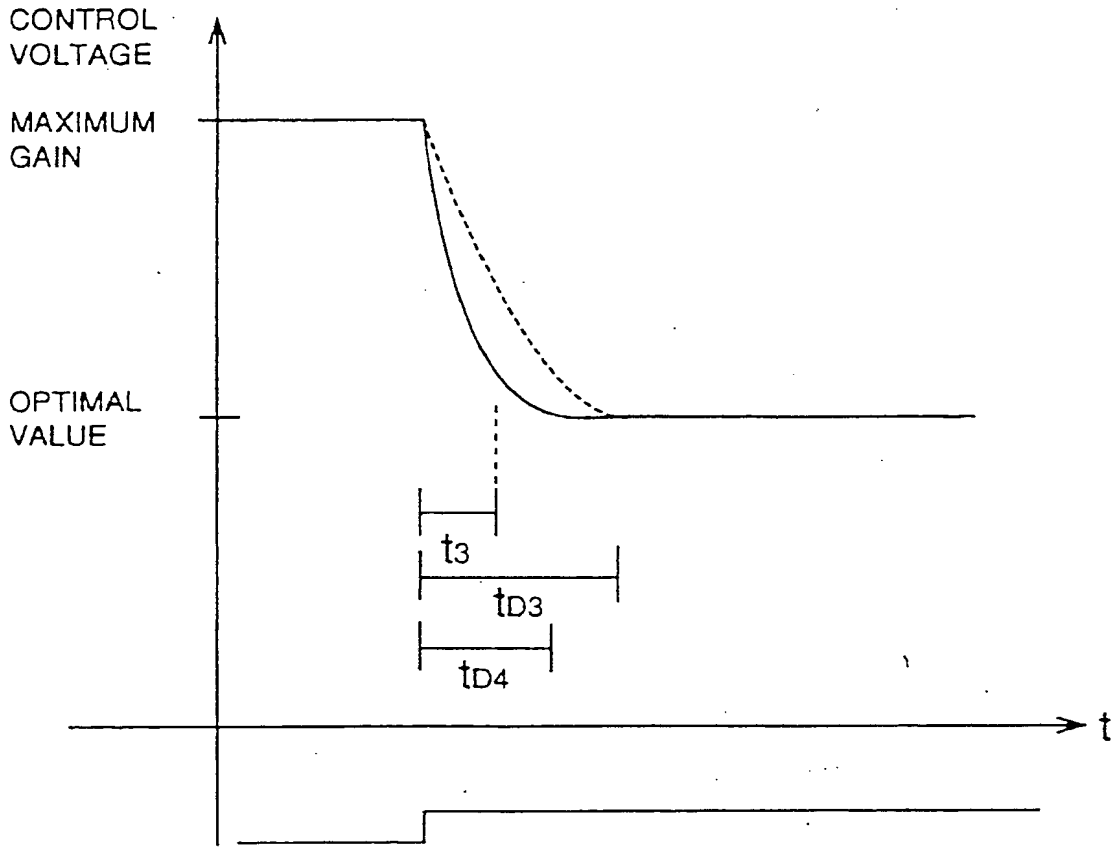
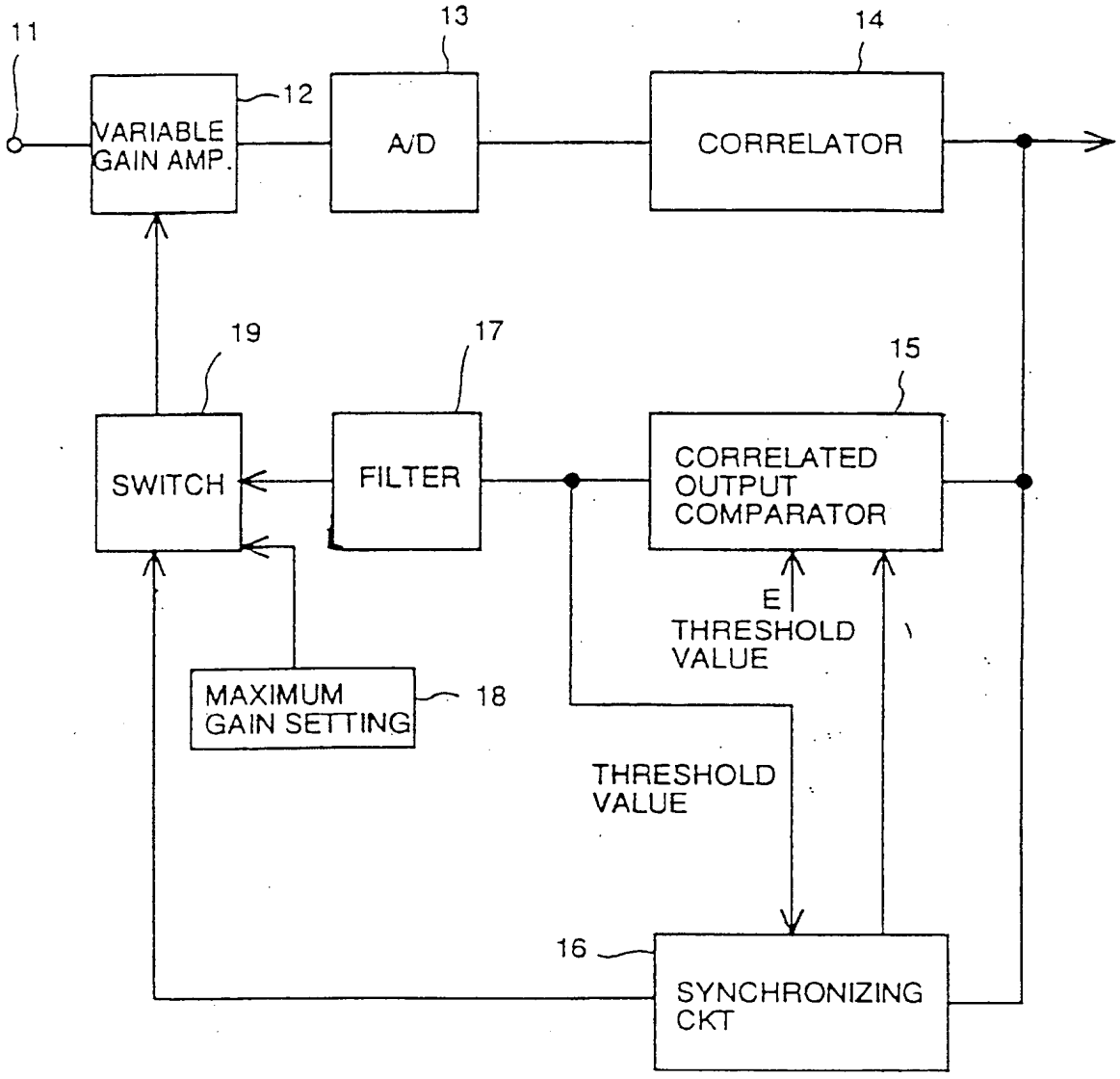


FIG. 13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VARIABLE GAIN AMP.
A/D
CORRELATOR
19
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15
SWITCH
FILTER
CORRELATED OUTPUT COMPARATOR
E
THRESHOLD VALUE
MAXIMUM GAIN SETTING
18
THRESHOLD VALUE
16
SYNCHRONIZING CKT

FIG. 14

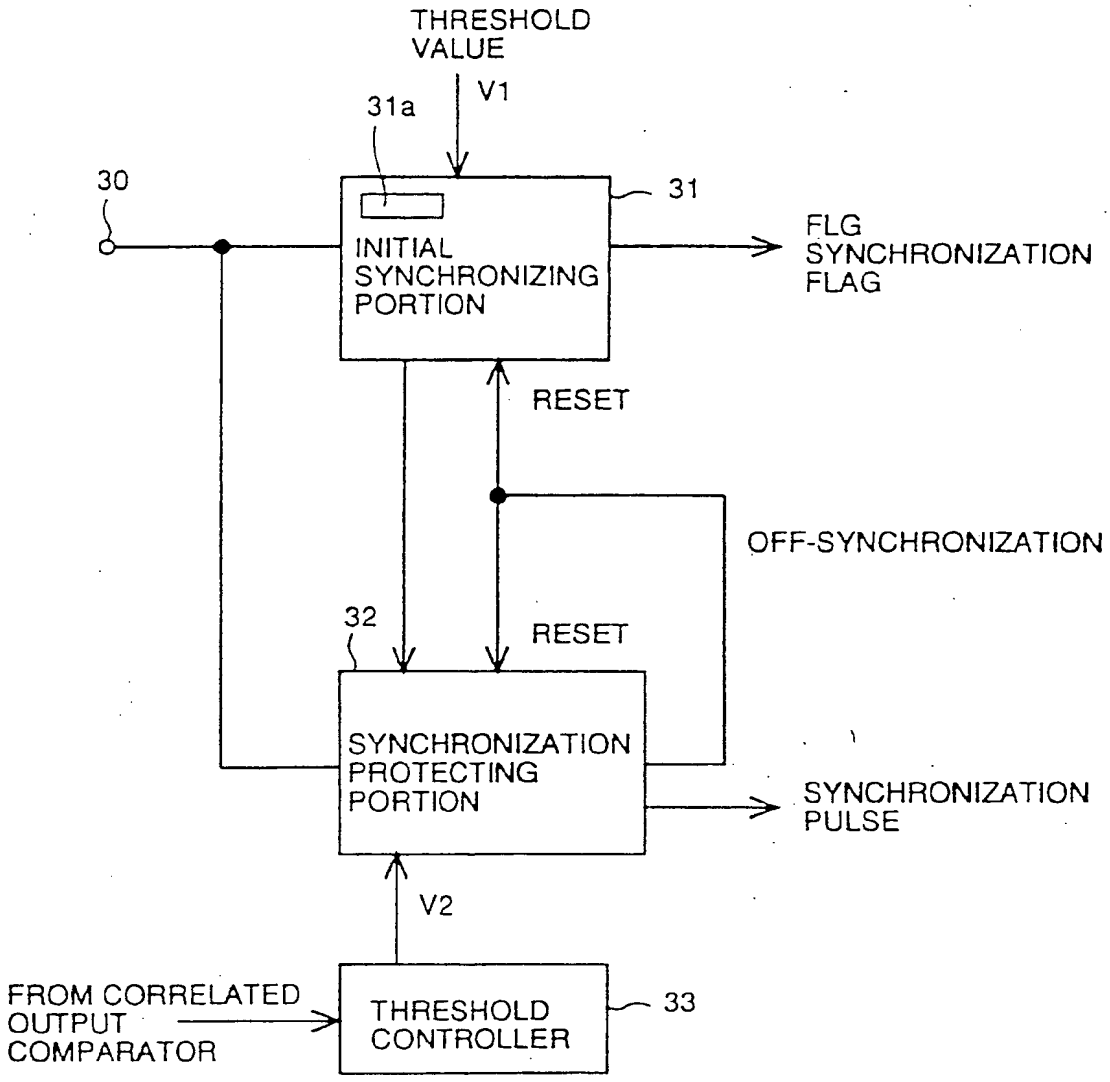
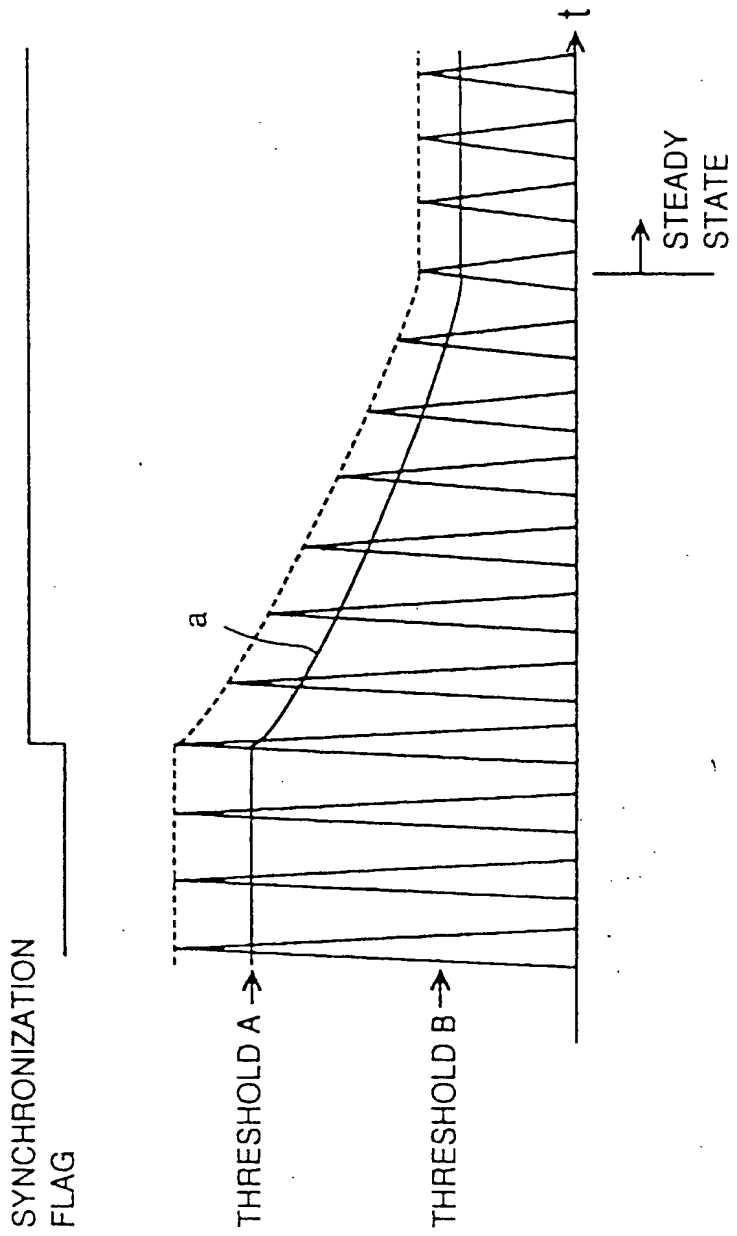


FIG. 15



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(71) Applicant: **SHARP KABUSHIKI KAISHA**
**Osaka-shi, Osaka-fu 545-0013 (JP)**

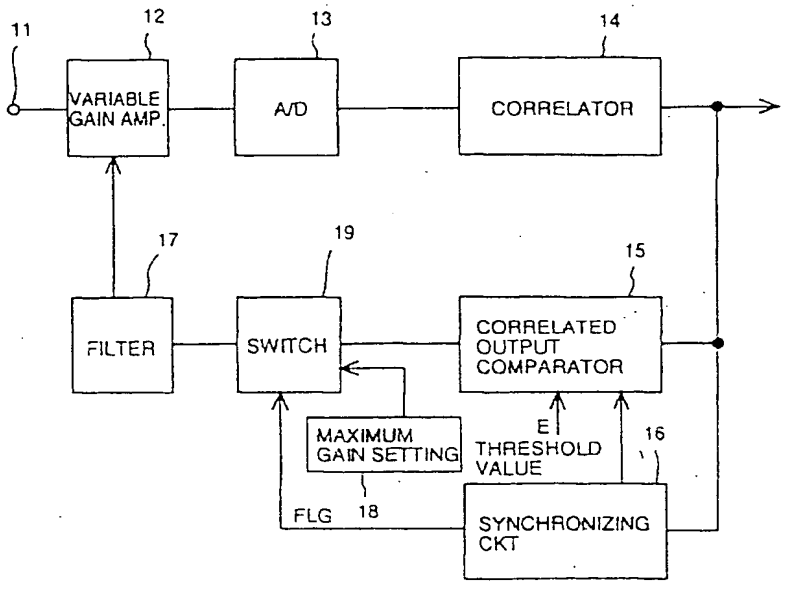
(72) Inventor: **Okamoto, Naoki**
**Chiba-shi, Chiba (JP)**

(74) Representative: **Brown, Kenneth Richard et al**
**R.G.C. Jenkins & Co.**
**26 Caxton Street**
**London SW1H 0RJ (GB)**

## (54) Spread spectrum signal receiver

(57) Amplitude level of a received signal is controlled by a variable gain amplifier (12), the received signal with the amplitude level controlled is converted to a digital signal by an A/D converter (13), and correlation or demodulation is established by a correlator (14) on the digital value. A correlated output comparator (15) compares an output signal from the correlator with a prescribed threshold value to establish correlated synchronization using the output signal from the correlator, performs initial synchronization using the comparison output, the output amplitude level of the variable gain amplifier (12) is controlled in accordance with an output amplitude from the correlator (14), and gain of the variable gain amplifier (12) is switched to the maximum value by a switch (19) dependent on presence/absence of a synchronization establishment signal from the correlation synchronizing circuit (16).

FIG. 4

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European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 97 30 0284

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| A | US 5 347 534 A (AKAZAWA SHIGEO ET AL)<br>13 September 1994 (1994-09-13)<br>* column 3, line 15 - line 47 *<br>* column 5, line 5 - line 68 *<br>* column 7, line 55 - line 61 * | 1-9 | H04B7/005<br>H03G3/30<br>H04B1/16 |
| P,X | PATENT ABSTRACTS OF JAPAN<br>vol. 1997, no. 04,<br>30 April 1997 (1997-04-30)<br>-& JP 08 335901 A (FUJITSU GENERAL LTD),<br>17 December 1996 (1996-12-17)<br>* abstract * | 1,2,7,9 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H04B
H03G

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 30 August 2000 | Heinrich, D |

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30-08-2000

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 5347534 A | 13-09-1994 | JP 1036224 A | 07-02-1989 |
| | | JP 2117422 C | 06-12-1996 |
| | | JP 8017341 B | 21-02-1996 |
| | | JP 1109925 A | 26-04-1989 |
| | | JP 2070160 C | 10-07-1996 |
| | | JP 7087397 B | 20-09-1995 |
| | | DE 3825740 A | 09-02-1989 |
| | | DE 3844767 C | 11-03-1993 |
| | | FR 2618959 A | 03-02-1989 |
| | | GB 2208462 A,B | 30-03-1989 |
| | | US 4899364 A | 06-02-1990 |
| JP 08335901 A | 17-12-1996 | NONE | |

EPO FORM P459

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